SWAMI VIVEKANAND UNIVERSITY, SIRONJA, SAGAR (M.P.)

SYLLABUS

For

M.Tech Electronics & Communication

Embedded System and VLSI Design

Semester I-IV

Swami Vivekanand University, Sironja Sagar
2014-2016

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

First Semester- Master of Technology

(Embedded System and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assignments /Quiz	End. Sem. Practical/ Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD-101	Advanced Mathematics	3	1	-	4	70	20	10	-	-	100
2.	MTVD-102	CMOS VLSI Design	3	1	-	4	70	20	10	-	-	100
3.	MTVD-103	Advanced Logic Design	3	1	-	4	70	20	10	-	-	100
4.	MTVD-104	Digital Signal Processing	3	1	-	4	70	20	10	-	-	100
5.	MTVD-105	Embedded Microcontroller Programming	3	1	-	4	70	20	10	-	-	100
6.	MTVD-106	Lab-I Embedded System Design (102, 105)	-	-	6	6	-	-	-	90	60	150
7.	MTVD-107	Lab-II Digital Design (103, 104)	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture - T: Tutorial - P: Practical

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

Second Semester- Master of Technology

(Embedded System and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assignments /Quiz	End. Sem. Practical/ Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD-201	VLSI Technology	3	1	-	4	70	20	10	-	-	100
2.	MTVD-202	Real Time Operating System	3	1	-	4	70	20	10	-	-	100
3.	MTVD-203	VLSI Test and Testability	3	1	-	4	70	20	10	-	-	100
4.	MTVD-204	Microelectronics	3	1	-	4	70	20	10	-	-	100
5.	MTVD-205	Embedded Computing System Design	3	1	-	4	70	20	10	-	-	100
6.	MTVD-206	Lab-I (Real Time Operating System)	-	-	6	6	-	-	-	90	60	150
7.	MTVD-207	Lab-II (VLSI Technology)	-	-	6	6	-	-	-	90	60	150
		Total	15	5	12	32	350	100	50	180	120	800

L: Lecture - T: Tutorial - P: Practical

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

Third Semester- Master of Technology

(Embedded System and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assignments /Quiz	End. Sem. Practical /Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD-301	Elective I	3	1	-	4	70	20	10	-	-	100
2.	MTVD-302	Elective II	3	1	-	4	70	20	10	-	-	100
3.	MTVD-303	Seminar	-	-	4	4	-	-	-	-	100	100
4.	MTVD-304	Preliminary Dissertation cum Synopsis	-	-	8	8	-	-	-	120	80	200
		Total	6	2	12	20	140	40	20	120	180	500

L: Lecture - T: Tutorial - P: Practical

MTVD 301 Elective -I	
(A)	Opto-Electronics Integrated Circuits
(B)	System On Chip (SOC) Design

MTVD 302 Elective -II	
(A)	Communication RF IC Design
(B)	Embedded System Programming

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

Fourth Semester- Master of Technology

(Embedded System and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments /Quiz	End Sem. Practical/Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD 401	Dissertation Part- II	-	-	20	20	-	-	-	300	200	500
		Total	-	-	20	20	-	-	-	300	200	500

L: Lecture - T: Tutorial - P: Practical

w.e.f. July-2013

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

Third Semester- Master of Technology

(Embedded System and VLSI Design,Micro electronics and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End. Sem. Exam.	Tests (Two)	Assignments /Quiz	End. Sem. Practical /Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD-301	Elective I	3	1	-	4	70	20	10	-	-	100
2.	MTVD-302	Elective II	3	1	-	4	70	20	10	-	-	100
3.	MTVD-303	Seminar	-	-	4	4	-	-	-	-	100	100
4.	MTVD-304	Preliminary Dissertation cum Synopsis	-	-	8	8	-	-	-	120	80	200
		Total	6	2	12	20	140	40	20	120	180	500

L: Lecture - T: Tutorial - P: Practical

MTVD 301 Elective -I	
(A)	Opto-Electronics Integrated Circuits
(B)	System On Chip (SOC) Design

MTVD 302 Elective -II	
(A)	Communication RF IC Design
(B)	Embedded System Programming

Swami Vivekanand University, Sagar (M.P.)

Scheme of Examination

Fourth Semester- Master of Technology

(Embedded System and VLSI Design)

S.No.	Subject Code	Subject Name	Periods per week			Credits	Maximum Marks (Theory Slot)			Maximum Marks (Practical Slot)		Total Marks
			L	T	P		End Sem. Exam.	Tests (Two)	Assignments /Quiz	End Sem. Practical/Viva	Practical Record/ Assignment/Quiz /Presentation	
1.	MTVD 401	Dissertation Part- II	-	-	20	20	-	-	-	300	200	500
		Total	-	-	20	20	-	-	-	300	200	500

L: Lecture - T: Tutorial - P: Practical

w.e.f. July-2013

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 101 Advanced Mathematics

UNIT I

Solution of Partial Differential Equation (PDE) by separation of variable method, numerical solution of PDE (Laplace, Poisson's, Parabola) using finite difference methods, Elementary properties of FT, DFT, WFT, Wavelet transform, Haar transform.

UNIT II

Probability, compound probability and discrete random variable. Binomial, Normal, Poisson's distribution, Sampling distribution, elementary concept of estimation and theory of hypothesis, recurred relations.

UNIT III

Stochastic process, Markov process transition probability transition probability matrix, just and higher order Markov process, Markov chain. Queuing system, transient and steady state, traffic intensity, distribution queuing system, concepts of queuing models (M/M/1: Infinity/ Infinity/ FC FS), (M/M/1: N/ Infinity/ FC FS), (M/M/S: Infinity/ Infinity/ FC FS)

UNIT IV

Operations of fuzzy sets, fuzzy arithmetic & relations, fuzzy relation equations, fuzzy logics, MATLAB introduction programming in MATLAB scripts, functions and their application.

UNIT V

Introduction and definition of reliability, derivation of reliability functions, Failure rate, Hazard rate, mean time t future & their relations, concepts of fault tolerant analysis, Elementary idea about decision theory and goal programming.

Reference Books:

1.Higher Engineering Mathematics by B.V. Ramana, Tata Mc Hill.
2. Advance Engineering Mathematics by Ervin Kreszig, Wiley Easten Edd.
3. Applied Numerical Methods with MATLAB by Steven C Chapra, TMH.
4. Introductory Methods of Numerical Analysis by S.S. Shastry,
5. Introduction of Numerical Analysis by Forberg
6. Numerical Solution of Differential Equation by M. K. Jain
7. Numerical Mathematical Analysis By James B. Scarborogh
8. Fourier Transforms by J. N. Sheddon
9. Fuzzy Logic in Engineering by T. J. Ross
10. Fuzzy Sets Theory & its Applications by H. J. Zimmersoms

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 102 CMOS VLSI Design

Unit I

VLSI design methodologies: VLSI Design flow, Design Hierarchy, Regularity, Modularity and Locality, VLSI design styles, Design quality, Packaging technology. MOS device design equations, Second order effects, the complementary CMOS Inverter DC characteristics.

Unit II

Circuit Characterization and Performance Estimation: Parasitic effect in Integrated Circuits, Resistance estimation, capacitance estimation, Inductance, Switching characteristics, CMOS Gate transistor sizing, Power dissipation, CMOS Logic Structures, Clocking Strategies.

Unit III

CMOS Process Enhancement and Layout Considerations: Interconnect, circuit Elements, Stick diagram, Layout design rules, Latchup, latchup triggering, latchup prevention, Technology related CAD issues.

Unit IV

Subsystem Design: Structured design of combinational logic- parity generator, Multiplexer, code converters, Clocked sequential circuits- two phase clocking, charge storage, dynamic register element, dynamic shift register, Subsystem design process, Design of ALU subsystem, Adders, Multipliers, Commonly used storage/ memory elements.

Unit V

Field Programmable Devices: Definitions of Relevant Terminology, Evolution of Programmable Logic Devices, User- Programmable Switch Technologies, Computer Aided Design (CAD) Flow for FPDs, Programmable Logic, Programmable Logic Structures, Programmable Interconnect, Reprogrammable Gate Array, Commercially Available SPLDs, CPLDs and FPGAs, Gate Array Design, Sea-of-Gates.

References

1. D.A. Pucknell, K. Eshraghian, *Basic VLSI Design*, PHI, 3rd Ed.
2. John P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley & Sons.
3. Niel H.E. Weste, K. Eshraghian,, *Principles of CMOS VLSI Design*, Person, 2nd Ed.
4. Mead and L. Conway, *Introduction to VLSI Systems,* Addison-Wesley.
5. A. Mukherjee, *Introduction to nMOS and CMOS VLSI systems design*, Prentice Hall

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 103 Advanced Logic Design

Unit I

Course overview; design concepts, introduction to logic circuit and Verilog. Implementation technology, CMOS logic gates, programmable logic devices. Optimized implementations of logic functions, canonical representations, Karnaugh maps, factoring, functional decomposition, NAND/NOR networks, bubble pushing.

Unit II

Verilog data types and operators, modules and ports, gate level modeling, time simulation/ scheduler. Circuit issues, Verilog behavioral models, number representation and arithmetic circuits, positional notation, signed numbers, arithmetic operations.

Unit III

Verilog specifications of combinational circuits, combinational logic building blocks, encoders/decoders, Multiplexers / Demultiplexers, Magnitude Comparator, arithmetic comparison.

Unit IV

The basic Latch and flip flop gated SR, JK,T and D Latch, Masterslave and edge.

Unit V

Synchronous sequential circuits, design process, state assignment, hazards, glitches, asynchronous design, Metastability, Noise margins, Power, fan-out, skew Finite state machine design examples, Verilog representations.

Reference Books

1. John F. Wakerly, *Digital Design*, Pearson Education Asia, 3rd Ed.
2. M. M. Mano, *Digital Design,* Pearson Education, 3rd Ed.
3. C. H. Roth, Jr., *Fundamentals of Logic Design*, Jaico Publishing House.
4. Fletcher, *An Engineering Approach to Digital Design*, PHI.
5. J. M. Yarbrough, *Digital Logic*, Thomson Learning.
6. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, McGraw-Hill Higher Education, 2003, ISBN 0-07-283878-7.
7. Samir Palnitkar, *Verilog HDL,* Prentice Hall, 2nd Edition, 2003, ISBN 0-13-044911

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 104 Digital Signal Processing

UNIT I

Introduction to Discrete Time Signals Sequences, representation of signals on orthogonal basis, Sampling and Reconstruction of signals.

UNIT II

Discrete Systems Attributes, Z-Transform, Analysis of LSI systems, Frequency analysis, Inverse systems, Discrete Fourier Transform (DFT), Fast Fourier Transform algorithms, Implementation of discrete time systems.

UNIT III

Design of FIR Digital Filters Window method, Park-McClellan's method, Effect of finite register length in FIR filter design.

UNIT IV

Design of IIR Digital Filters Butterworth, Chebyshev and Elliptic Approximations; Lowpass, Bandpass, Bandstop and High pass filters.

UNIT V

Introduction to VLSI DSP Transformations for high speed using pipelining, retiming, parallel processing, and folding techniques; Design of programmable DSPs.

References

1. A.V. Oppenheim and Schafer, *Discrete Time Signal Processing*, Prentice Hall, 1989.
2. John G. Proakis and D.G. Manolakis, *Digital Signal Processing: Principle, Algorithms and Applications*, Prentice Hall, 1997.
3. L.R. Rabiner and B. Gold, *Theory and Application of Digital Signal Processing*, Prentice Hall, 1992.
4. J.R. Johnson, *Introduction to Digital Signal Processing*, Prentice Hall, 1992.
5. D. J. DeFatta, J. G. Lucas and W. S. Hodgkiss, *Digital Signal Processing*, J Wiley and Sons, Singapore, 1988.
6. K.K. Parhi, *VLSI Digital Signal Processing Systems: Design and Implementation*, Wiley.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 105 Embedded Microcontrollers Programming

Unit-I

Embedded System Overview: Embedded System definition.

Processor Technology: General purpose, Single Purpose, Application Specific, Super scalar, Pipelined, Very Long Instruction Word (VLIW) Processor, Microprocessors, Micro controllers and DSP Processors. Embedded Processors in VLSI circuit.

Unit-II

Architectural Issues: CISC, RISC, DSP and Harvard/Princeton Architectures. Memory: ROM, EPROM, EEPROM, FLASH, RAM, SRAM, DRAM, SDRAM, NVRAM, EDORAM, DDRRAM, Memory Hierarchy and Cache.

Interfacing: Interfacing using Glue Logic, Interrupt, DMA, I/O Bus structure, I/O devices, Serial Communication Protocols, Parallel Communication Protocols, Wireless Protocols.

Unit-III

Introduction to 8-bit Microcontrollers e.g. 8051, 68HC11, 80196, Timers/Counters, USART. Detailed study of 8051 microcontroller, with its programming in assembly language and Interrupts, Serial Programming etc.

Unit-IV

Interfacing of Microcontroller such as SPI, PWM, WDT, Input Capture, Output Compare Modes, Interfacing LED, Switches, ADC, DAC, LCD, RTC. Idea about the C programming of Microcontroller, I2C, CAN bus architecture.

Unit-V

Introduction to 16/32-bit microcontrollers, Introduction to ARM Architecture and Organization, Difference between ARM7, ARM9 & ARM11 TDMI, ARM programming model, ARM Instruction set.

References

1. David E. Simon, *An Embedded Software Primer*, Pearson Education.
2. Dr. RajKamal, *Embedded Systems*, TMH.
3. Vahid & Givargis, *Embedded System Design*,John Wiley & Sons.
4. K. J. Ayala, *8051 Microcontrollers*, Penram International, Second Edition
5. M. A. Mazidi & J. G. Mazidi, *8051 Microcontroller and Embedded System,* Pearson Education Asia
6. J. W. Valvano, *Embedded Microcomputer Systems - Real Time Interfacing*, Thomson Asia Pte. Ltd.
7. R. H. Barnett, *8051 family of Microcontrollers,* PHI.
8. Peter Spasov, *Microcontroller Technology: The 68HC11*, PHI, Fourth Edition
9. Dr. Rajkamal, *Microcontrollers (Architecture, Programming, Interfacing and System Design),* Pearson Education.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 201 VLSI Technology

Unit I

Overview of Semiconductor Processing: Electronic grade silicon preparation, Crystal growth, Czochralski process, wafer-preparation, slicing, Marking, polishing, evaluation, Basic wafer fabrication operations, wafer sort, clean room construction and maintenance.

Unit II

Oxidation: Objectives, Silicon dioxide layer uses, Thermal oxidation mechanism and methods, Kinetics of oxidation, Deal Grove model, Oxidation processes, post oxidation evaluation.

Unit III

Basic Patterning: Photo-masking process, Ten step process, Basicphotoresist chemistry, comparison of positive and negative photo resists, X-ray lithography, Electron beam exposure system.

Unit IV

Doping: Definition of a junction, Formation of doped region and junction by diffusion, diffusion process steps, deposition, drive-in-oxidation, Ion implantation- concept and system, implant damage, Comparison of diffusion and ion-implantation techniques.

Unit V

Deposition: Chemical Vapor Deposition (CVD), CVD Process steps, CVD System types, Low- Pressure CVD (LPCVD), Plasma-enhanced CVD (PECVD), Vapor Phase Epitaxy (VPE), Molecular Beam Epitaxy (MBE), Metal organic CVD (MOCVD), SOS (Silicon on Sapphire) and SOI (silicon on Insulator). Brief Introduction to Metallization.

Text/ References

1. S.M. Sze, *VLSI Technology*, McGraw-Hill, 2nd Ed.
2. S. K. Gandhi, *VLSI Fabrication Principles*, Wiley
3. W. R. Runyan, *Silicon Semiconductor Technology*, McGraw-Hill.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 202 Real Time Operating System

Unit-I

Introduction to OS, Process Management & amp, Inter Process Communication, Memory management, I/O subsystem, File System Organization.

Unit-II

(i) Real Time Systems Concepts: Foreground/Background Systems, Critical Section of Code, Resource, Shared resource, Multitasking, task, context switch, Kernel, Schedules, Premptive & amp, Non-Premptive Kernel, various scheduling methods.

(ii) Real Time Scheduling. Real-Time task scheduling-Clock-driven, Event-driven, Scheduling of real-time task on auniprocessor, Rate Monotonic Analysis (RMA), Earliest Deadline First (EDF), Scheduling with limited priority levels.

Unit-III

Kernel structure, Task scheduling, Task management, Resource sharing among tasks, Priority inversion problem, Priority inheritance protocol, An overview of scheduling in multiprocessor and distributed systems.

Unit-IV

Performance Metrics of RTOS, Programming in VxWorks, or COS-II Overview of C/OS-II Overview of some other commercial embedded operating systems: PSOS, VRTX, RT Linux, WinCE.Benchmarking real-time operating systems.

Unit-V

Commercial real-time operating systems:Unix as areal-time operating system, Windows as a real-time operating system,Extensions to Unix : Host target approach,Preemption points,Fully preemptable kernel.

Text/References

1. Jean J. Labrosse, M*icroC/OS-II, The Real Time Kernel*
2. VxWorks details from Internet.
3. C/OS-II Manuals
4. David E. Simon, A*n Embedded Software Primer,* Pearson Education
5. Dr. Rajib Mall, *Real time Systems, Theory and practices,* Pearson Education.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD-203 VLSI TEST AND TESTABILITY

Unit-I

Introduction to Testing Process: CMOS Testing, Reliability, Failures & Faults, Levels of Testing, Test economics, Elementary Testing Concepts, System and Field Testing, Burn in boards.

Unit-II

Logic Simulation & Fault modelling: Delay Models, Event driven simulation, general fault simulation, fault detection and redundancy, fault equivalence and fault dominance, Stuck-at faults, bridging faults, transistor faults, delay faults, Fault detection using Boolean Difference, Path Sensitization, Fault Collapsing.

Unit-III

Test generation for combinational & sequential circuits: D-algorithm, PODEM, SPOOF, Automatic Test Pattern Generation, Primitive and Propagation Cubes, Fan-out Oriented Test Generation, Controllability and Observability, Testing of sequential circuits as iterative combinational circuits, state table verification, random testing.

Unit-IV

Design for testability: Ad-hoc methods, Full scan & Partial scan design,Boundary scans,Testability analysis.

Unit-V

Built-in self-test & IDDQ testing: RAM BIST, Logic BIST Random and weighted random pattern testability BIST Pattern generator and response analyzer Scan-based BIST architecture Test point insertion for improving random testability, IDDQ testing, IDDQ test patterns, IDDQ measurement Case studies, Design for IDDQ testability.

Reference:

1. Parag K. Lala, *Fault Tolerant and Fault Testable Hardware Design*, BS Publication.
2. N. Weste and K. Eshraghian, *Principles of CMOS VLSI design,* Addison-Wesley.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 204 Micro Electronics

Unit I

Review of quantum mechanics theory. Motion of electron in a periodic lattice. Band theory of solids, effective mass, holes.

Unit II

Statistics of carriers in semiconductors. Lifetime and recombination theory. Boltzmann transports equation. Carrier transport in semiconductors, including high field effect.

Unit III

P-N junction theory. Excess currents and breakdown in p-n junctions. Bipolar transistors. Ebers-Moll and small signal models. Switching characteristics. No uniformly doped transistors. High current and high frequency effects.

UNIT IV

FET construction -construction ,N channel P- channel , characteristics ,parameters ,equivalent modelend voltage gain , enhancement and depletion MOSFET and its characteristics , analysis of FET , in various configuration.

UNIT V

Oscillator: Condition of sustained oscillation, RC phase shift .LC Hartley and collpit , oscillator Wien bridge , negative resistance ,(tunnel diode and UJT) oscillator , crystal oscillator

References

1. J.L. Moll, *Physics of Semiconductors,* McGraw Hill
2. F.Y. Wang, *Introduction to Solid State Electronics,* North Holland.
3. S.M. Sze, *Physics of Semiconductor Devices*, Weiley Easter.
4. D.J. Roulston, *Dipolar Semiconductors Devices*, McGraw Hill
5. R.L. Pritchnard, *Electrical Characteristics of Transistors*, McGraw Hill

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 205 Embedded Computing System Design

Unit-I

Introduction: Embedding Complex Systems and Microprocessors Embedded System Design Process, Designing Hardware and Software Components, Formalization of System Design, Application Examples.

Unit-II

Instruction Sets: Assembly Language, ARM processor and memory organization. Data Operations and Control of Flow, SHARC Processor, Memory organization, Data Operations and flow control, Parallelism within the instructions.

Unit-III

CPUs: Performance, Power Dissipation, Design Example, Data Compression, CPU Bus Protocols in ARM, Design, Development and Debugging.

Unit-IV

Program design and Analysis: Program Design, Models of Program, Assembling, Linking, Compiling, Analysis and optimization of the Program Size and Execution times, Design Example: Software Modem.

Unit-V

System Design Techniques: Design Methodologies, Requirement Analysis, specifications, System Analysis, quality Assurance, Two Design Examples in Networking and Internet Enabled Systems and Automobile Applications.

Reference:

Wayne Wolf, *Computers as Components,* Harcourt India Private Ltd.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD – 301(A) Opto-Electronics Integrated Circuits

Unit I

Theory of Optical Wave guides: Wave guide theory : one dimensional planar wave guides, two dimensional wave guides, transcendental equations, wave guide modes, mode cutoff conditions.

Unit II

Optical Wave guide Fabrication and Characterization: Waveguide fabrication: deposited films; vacuum-deposition and solution-deposition, diffused waveguides, ion-exchange and ion-implanted waveguides, epitaxial growth of III-V compound semiconductor materials, shaping of waveguides by wet and dry etching techniques. Waveguide characterization: surface scattering and absorption losses, radiation and bending losses, measurement of waveguide loss, waveguide profiling.

Unit III

Fundamentals of Optical Coupling: Transverse couplers. Prism couplers. Grating couplers. Fiber to waveguide couplers. Coupling between optical waveguides. Directional couplers. Applications of directional couplers.

Unit IV

Guided Wave Modulators and Switches: Physical effects used in light modulators : electro-optic, acousto-opticand magneto-optic effects. Waveguide modulators and switches.

Unit V

Semiconductor Lasers and Detectors: Laser diodes. Distributed feedback lasers. Integrated optical detectors.

Recent Progress in Integrated Optics: State-of-the-art technology in guided wave devices and applications, e.g. photonic switching, tunable laser diodes, optical integrated circuits.

Reference

1. T Tamir, *Guided Wave Optoelectronics,* Springer-Verlag, 1990
2. R Sysm & J Cozens, *Optical Guided Waves and Devices*, McGraw-Hill, 1993

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD 301 (B) - System on Chip (SOC) Design

UNIT I

Recent advances in semiconductor technology, Programmable logic devices, such as field programmable gate arrays (FPGAs), Programmable chip architectures, logic synthesis, SoC concepts, and the Verilog synthesizable subset, Implementation of a complex system on a single programmable chip.

UNIT II

Tools and techniques for designing, verifying and implementing System-on-Chip (SoC) designs using programmable logic. Embedded system applications and their system-level hardware-software co-design.

UNIT III

Implementation Aspects: Adders, ALUs, Multipliers, Dividers, Register Files, Buses, CISC/RISC, Memory hierarchy (caches, MMU, main memory)

UNIT IV

ARM System-on-chip architecture, memory management support (MMU), Highest performance at low power, Protected memory (MPU), Low latency and predictability.

UNIT V

Project Orientation: Concept to Verilog hardware description language (HDL), verification using simulation, synthesis and programmable device implementation on an FPGA development board.

Reference

1. Palnitkar, Samir, Verilog HDL, Prentice Hall, 2003, 2nd Ed., ISBN 0-13-044911-3
2. Bhasker, J., Verilog HDL Synthesis – A Practical Primer, Star Galaxy Publishing, Allentown PA, 1998, ISBN 0-9650391-5-3
3. Maxfield, Clive, The Design Warrior's Guide to FPGAs, Newnes, 2004, ISBN 0-7506-7604-3
4. Smith, D. J., HDL Chip Design, Doone Publications, Madison AL, 1999, ISBN 0-9651934-3-8
5. Sutherland, Stuart, Verilog 2001 – A Guide to the New Features of the Verilog Hardware
6. Description Language, Kluwer Academic Publishers, 2002, ISBN 0-7923-7568-8
7. Cummings, C., Nonblocking Assignments in Verilog Synthesis, Coding Styles That Kill, Synopsys Users Group 2000
8. Cummings, C., "full_case parallel_case", the Evil Twins of Verilog Synthesis, Synopsys Users Group 1999
9. Mills, D., Cummings, C., RTL Coding Styles That Yield Simulation and Synthesis Mismatches, Synopsys Users Group 1999
10. Xilinx Spartan-3 FPGA Family Data Sheet, DS099-2
11. Xilinx PicoBlaze KCPSM3 Microcontroller Users Manual

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD 302 (A) - Communication RF IC Design

Unit I

Basic concepts in RF Design: Analysis & Measurement Techniques. S-Parameter Models, Smith Chart Calculations.

Unit II

Trans-receiver Architecture for Wireless Communication Standards. Non-Linearity, Harmonics, Gain Compression, Desensitization, Cross Modulation, IMD & Inter-symbol Interface.

Unit III

RF IC Design concepts & Device Technologies: Low Noise Amplifiers, Mixers, Frequency Sources, Oscillators & Synthesizers, Power Amplifiers. Noises & Distortions in LNA, PA & Mixer Circuits.

Unit IV

PLL: Theory, Circuits, Distortion & Noises. Microwave Circuit Components & Design Concepts: Single Chip Radio Concepts, Design Issues Surrounding Systems as DECT, GSM, Blue Tooth etc. Case Studies.

UNIT V

Impedance matching using discrete components micro strip line ,matching network , single stub matching network, Double stub matching networks ,quarter wave transformers , multi section and tapered transformers.

Reference

1. Behzad Razavi, *RF Microelectronics*, PHI 1998.
2. R. Ludwig & P. Bretchko, *RF Circuit Design,* PHI 2000.
3. L.E. Larson, *RF & Microwave Circuit Design for Wireless Communication,* Artech House Publishers, 1997.
4. Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits*, Cambridge University Press, 1998.
5. George Vendelin, *Design of Amplifiers & Oscillators by S-Parameter Method,* J. Wiley & Sons, 1982.

SWAMI VIVEKANAND UNIVERSITY, SAGAR (M.P.)

MTVD 302 (B) Embedded System Programming

Unit-I

Introduction to Linux Operating System. Shell Programming, Review of C-Programming and Data Structures.

Unit-II

Overview of Embedded Systems – Sequential and Concurrent Models – Processor Solutions and Types – Types of Memory – Data Representation Formats – Usage of C in Embedded Systems – Programmers view of CPU – IO programming models – Concurrent Software Design – Scheduling – Memory Management – Mixing C & Assembly.

Unit-III

Embedded System Design Issues , Challenges & Trends in Embedded Systems, Assemblers, Compilers, Linkers, Loaders, Debuggers, Profilers & Test Coverage Tools, Utilities like make, ranlib, objcopy & objdump etc.

Unit-IV

Writing device drivers, Writing Time & Space Sensitive Programs, Programming in C for 8051, 68HC11 and 80196 microcontrollers.

UNIT-V

Advanced micro controllers: only brief general architecture of AVR,PIC ,and ARM micro controllers, JTAG concept and boundary scane Architecture.

References

1. David E. Simon, An Embedded Software Primer, Pearson Education.
2. Michel Barr, Programming Embedded Systems in C & C++, Shroff Publishers & Distributors Pvt. Ltd.
3. Frank Vahid and Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, John Wiley & Sons, 2002.
4. Daniel W. Lewis, Fundamentals of Embedded Software: Where C and Assembly Meet, Prentice Hall, 2002.
5. Jane Liu, Real-time Systems, Prentice Hall, 2000.